Single Step Pendeo- and Lateral Epitaxial Overgrowth of Group III-Nitride Epitaxial Layers with Group III-Nitride Buffer Layer and Resulting Structures

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Field of the Invention

The present invention relates to electronic device structures and fabrication methods, and more particularly to Group III-nitride semiconductor structures and methods of fabrication by pendeo- and lateral epitaxial overgrowth.

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Background

Gallium nitride (GaN) is a wide-bandgap semiconductor material widely known for its usefulness as an active layer in blue light emitting diodes. GaN is also under investigation for use in other microelectronic devices including laser diodes and high-speed, high power transistor devices. As used herein, "gallium nitride" or "GaN" refers to

15   gallium nitride and III-nitride alloys thereof, including aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN) and aluminum indium gallium nitride (AlInGaN).

High-quality bulk crystals of GaN are currently unavailable for commercial use. Thus, GaN crystals are typically fabricated as heteroepitaxial layers on underlying non-

20   GaN substrates. Unfortunately, GaN has a considerable lattice mismatch with most suitable substrate crystals. For example, GaN has a 15% lattice mismatch with sapphire and a 3.5% lattice mismatch with silicon carbide. Lattice mismatches between a substrate and an epitaxial layer cause threading dislocations which may propagate through the growing epitaxial layer. Even when grown on silicon carbide with an

25   aluminum nitride buffer layer, a GaN epitaxial layer exhibits dislocation densities estimated to be in excess of $10^8/cm^2$. Such defect densities limit the usefulness of GaN in highly sensitive electronic devices such as laser diodes.

Lateral Epitaxial Overgrowth (LEO) of GaN has been the subject of considerable interest since it was first introduced as a method of reducing the dislocation densities of

30   epitaxially grown GaN films. Essentially, the technique consists of masking an underlying layer of GaN with a mask having a pattern of openings and growing the GaN

up through and laterally onto the mask. It was found that the portion of the GaN layer grown laterally over the mask exhibits a much lower dislocation density than the underlying GaN layer or the portion of the GaN layer above the mask openings. As used herein, "lateral" or "horizontal" refers to a direction generally parallel to the surface of a substrate, while the term "vertical" means a direction generally orthogonal to the surface of a substrate.

One drawback to conventional LEO techniques is that separate process steps are required for growing the underlying GaN layer, masking the GaN layer and then growing the lateral layer. Early embodiments of LEO did not place the mask directly on the non-GaN substrate because unwanted nucleation would occur on the mask during nucleation of the GaN layer at low temperatures, preventing adjacent laterally-grown regions from coalescing (or otherwise from growing laterally a desired distance if coalescence is not required). When the mask is placed directly on a GaN layer, unwanted nucleation on the mask is typically not a problem since low temperature nucleation is not required and the growth temperature of GaN is very high, typically above 1000°C. During high temperature growth, unwanted nucleation does not occur on the mask due to the much higher sticking coefficient of gallium atoms on the gallium nitride surface as compared to the mask.

This drawback is addressed with some success by a "single step" process for LEO. Shealy et al. disclosed a process whereby an underlying SiC or sapphire substrate was masked with silicon nitride. The process is referred to as "single step" because it does not require growth of an intermediate layer of GaN between the substrate and the mask. Shealy found that minimizing nucleation on the silicon nitride mask permitted growth of a relatively defect free layer of laterally-grown GaN over the masks. However, under certain circumstances it is desirable to avoid having to minimize nucleation on the mask, yet still be able to grow a relatively defect free layer of GaN in a single step process.

Object and Summary of the Invention

Accordingly, there is a need in the art for a method of fabricating a relatively defect-free single crystal film of gallium nitride in a single step process without having to minimize nucleation on the mask layer.

Moreover, there is a need in the art for a method of fabricating a relatively defect-free single crystal film of gallium nitride in a single step process without having to minimize nucleation on the mask layer which provides a conductive buffer layer to permit electrical communication between a conductive substrate and an epitaxial layer of gallium nitride.

It is an object of the present invention to provide a method of fabricating a relatively defect-free single crystal film of gallium nitride in a single step process without having to minimize nucleation on the mask layer.

It is a further object of the present invention to provide a method of fabricating a relatively defect-free single crystal film of gallium nitride in a single step process without having to minimize nucleation on the mask layer which provides a conductive buffer layer to permit electrical communication between a conductive substrate and an epitaxial layer of gallium nitride.

The foregoing and other objects are achieved by a method of fabricating a gallium nitride-based semiconductor structure on a substrate. The method includes the steps of forming a mask having at least one opening therein directly on the substrate, growing a buffer layer through said at least one opening, and growing a layer of gallium nitride upwardly from said buffer layer and laterally across said mask. During growth of the gallium nitride from the mask, the vertical and horizontal growth rates of the gallium nitride layer are maintained at rates sufficient to prevent polycrystalline material nucleating on said mask from interrupting the lateral growth of the gallium nitride layer.

In an alternative embodiment, the method includes forming at least one raised portion defining adjacent trenches in the substrate and forming a mask on the substrate, the mask having at least one opening over the upper surface of the raised portion. A buffer layer may be grown from the upper surface of the raised portion. The gallium nitride layer is then grown laterally by pendeoepitaxy over the trenches.

In another embodiment, the present invention provides a gallium nitride-based semiconductor structure on a substrate. The structure includes a substrate and a mask having at least one window therein applied directly on the upper surface of the substrate. An overgrown layer of gallium nitride extends upwardly from the mask window and laterally across the mask, on which polycrystalline material has nucleated and grown.

In another embodiment, the substrate includes at least one raised portion defining adjacent trenches. A mask structure overlays the substrate and a window in the mask exposes at least a portion of the upper surface of the raised portion. An overgrown layer of gallium nitride extends upwardly from the mask window and laterally over the trench and across the mask, on which polycrystalline material has nucleated and grown.

Brief Description of the Drawings

FIG. 1 is a cross-section of a substrate on which a mask has been patterned.

FIG. 2 is a plan view of a substrate on which a mask has been patterned.

FIG. 3 is a cross section of a substrate on which a layer of GaN has been epitaxially grown by LEO on a conductive buffer layer.

FIG. 3A is a cross section of a substrate on which a layer of GaN is being epitaxially grown by LEO on a conductive buffer layer, but has not coalesced.

FIG. 4 is a cross section of a substrate on which excessive nucleation on the mask has interrupted the lateral growth of a layer of GaN.

FIG. 5 is a cross section of a substrate on which a layer of GaN has been epitaxially grown in accordance with an aspect of the present invention.

FIG. 6 is a cross section of a substrate on which a layer of GaN has been epitaxially grown in accordance with another aspect of the present invention.

FIG. 6A is a cross section of a substrate on which a pair of raised portions has been formed and a mask layer has been deposited.

FIG. 6B is a cross section of a substrate on which a pair of raised portions has been formed and a mask layer has been deposited using a self-alignment technique.

FIG. 7 is a cross-sectional SEM image showing the interruption of lateral growth of a GaN layer by crystals nucleating on the mask.

FIG. 8 is a plan view SEM image of two GaN stripes in which crystallites on the underlying mask disturbed the epitaxial growth.

FIG. 9 is a cross-sectional SEM of GaN stripes grown in accordance with an embodiment of the present invention using a reflective mask layer.

FIG. 10 is a cross-sectional SEM of GaN stripes grown in accordance with an embodiment of the present invention until adjacent regions have coalesced over the reflective masks.

FIG. 11 is a cross-sectional SEM of a GaN layer grown on a conductive buffer layer over a Si_3N_4 mask.

FIG. 12 is a cross sectional SEM of a GaN layer grown in accordance with a second embodiment of the present invention.

FIG. 13 is a plan view SEM image of two GaN stripes grown in accordance with the second embodiment of the present invention.

FIG. 14 is a cross-sectional TEM (Transmission Electron Microscopy) image of a layer of GaN grown in accordance with the present invention.

FIG. 15 is a cross-sectional SEM of GaN stripes grown in accordance with an embodiment of the present invention while maintaining a ratio of lateral to horizontal growth rates of 4.2:1.

FIG. 16 is a cross-sectional SEM of GaN stripes grown in accordance with an embodiment of the present invention while maintaining a ratio of lateral to horizontal growth rates of 1:1.

Detailed Description of the Invention

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and regions illustrated in the figures are illustrated schematically. As will also be appreciated by those of skill in the

art, references herein to a layer formed "on" a substrate or other layer may refer to the layer formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer. References herein to a layer formed "directly on" a substrate or other layer refer to the layer formed on the substrate without an intervening

5   layer or layers formed on the substrate or other layer. The present invention is not limited to the relative size and spacing illustrated in the accompanying figures.

Basic LEO techniques are described in A. Usui, et al., "Thick GaN epitaxial growth with low dislocation density by hydride vapor phase epitaxy," Jpn. J. Appl. Phys. Vol. 36, pp. L899-902 (1997). Various LEO techniques including pendeoepitaxial

10   techniques are described in U.S Application Serial No. 09/032,190 "Gallium Nitride Semiconductor Structures Including a Lateral Gallium Nitride Layer that Extends From an Underlying Gallium Nitride Layer", filed February 27, 1998; Application Serial No. 09/031,843 "Gallium Nitride Semiconductor Structures Including Laterally Offset Patterned Layers", filed February 27, 1998; Application Serial No. 09/198,784,

15   "Pendeoepitaxial Methods of Fabricating Gallium Nitride Semiconductor Layers on Silicon Carbide Substrates by Lateral Growth from Sidewalls of Masked Posts, and Gallium Nitride Semiconductor Structures Fabricated Thereby" filed November 24, 1998; and Application Serial No. 60/088,761 "Methods of Fabricating Gallium Nitride Semiconductor Layers by Lateral Growth from Sidewalls into Trenches, and Gallium

20   Nitride Semiconductor Structures Fabricated Thereby," filed June 10, 1998, the disclosures of each of which are hereby incorporated herein by reference.

Referring now to FIG. 1, a substrate 10 is illustrated on which is deposited a mask layer 14 comprising stripes 14a and 14b. Although the stripe pattern may continue in a periodic or aperiodic fashion on either side, for convenience only stripes 14a and 14b are

25   illustrated. Stripes 14a, 14b are characterized in that they have a width (w) and are separated by mask openings or windows 6 having a window length (l). The distance between an edge of stripe 14a and the corresponding edge of stripe 14b is defined as the period (p) of the mask pattern, at least with respect to stripes 14a and 14b, such that p=w+l.

30   The mask layer may be deposited using plasma enhanced chemical vapor deposition (PECVD), sputtering, electron-beam deposition, thermal oxidation or other

deposition techniques, and patterned using standard photolithographic techniques. The PECVD process is described in detail in Chapter 6 of S.M. Sze, *VLSI Technology*, 2nd ed., McGraw-Hill 1988. Photolithographic techniques are well known in the art.

As illustrated in FIG. 2, stripes 14a and 14b are preferably oriented along the 5 $<1\bar{1}00>$ crystallographic direction in the (0001) plane. (Crystallographic designation conventions used herein are well known in the art and need not be described further.) The mask layer 14 may comprise silicon nitride (Si_xN_y) or silicon dioxide (SiO_2) or any other suitable mask material. If the structure being fabricated is intended for use in an optical device such as an LED or laser diode, the mask layer 14 may comprise a 10 reflective or refractory metal which is stable in ammonia and hydrogen gas, has a melting point in excess of about 1200°C, and is reflective to the desired wavelength. Examples of such metals include tungsten (W) and platinum (Pt). Alternatively, the mask layer could comprise a Bragg reflector which may comprise alternating layers of Si_xN_y and SiO_2 or other oxides, the design of which is well known in the art.

15 The substrate may be silicon carbide, sapphire (Al_2O_3), silicon, ZnO, or any other similarly suitable substrate. Silicon carbide substrates are advantageous for a number of reasons. Silicon carbide provides closer lattice and thermal expansion matches for GaN, is thermally and chemically stable, has natural cleave planes, high thermal conductivity, and is transparent to visible wavelengths up to 380 nm. Also, silicon carbide has a 20 distinct advantage in that it is conductive, which permits fabrication of vertical-geometry devices. Silicon carbide substrates may have a polytype of 4H, 6H, 3C or 15R. Preferably, however, the substrate is 6H-SiC (on-axis).

The fabrication of substrate 10 is well known to those in the art. Fabrication of silicon carbide substrates are described, for example, in U.S. Patents 4,865,685 to 25 Palmour et al., Re34,861 to Davis, et al., 4,912,064 to Kong et al., and 4,946,547 to Palmour et al., the disclosures of each of which are hereby incorporated by reference. The fabrication of sapphire and silicon substrates is well known in the art and need not be described in detail.

Referring now to FIG. 3, an epitaxial layer 20 may be fabricated by first growing 30 a buffer layer 12 on the surface of the substrate 10. Epitaxial layer 20 may comprise gallium nitride or a Group III-nitride alloy thereof, such as aluminum gallium nitride

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(AlGaN), indium gallium nitride (InGaN), or aluminum indium gallium nitride (AlInGaN). For a SiC substrate, the buffer layer preferably comprises a layer 12 of $Al_xGa_{1-x}N$, where x represents the mole fraction of aluminum present in the alloy and $0 < x \leq 1$. In the case of silicon carbide substrates, the buffer layer 12 may have the structure

5   described in copending and commonly assigned U.S. Patent Application Serial No. 08/944,547 entitled "Group III Nitride Photonic Devices on Silicon Carbide Substrates with Conductive Buffer Interlayer Structure," filed October 7, 1997, the disclosure of which is hereby incorporated herein by reference.

Preferably, the topmost buffer layer comprises a mole percentage of Al of

10   between 9% and 12%, and is approximately 1000 to 5000 Å thick. The buffer layer 12 may be made conductive to the SiC substrate by the formation of capped GaN dots on the SiC substrate as described in U.S. Patent Application Serial No. 08/944,547 prior to the deposition of the buffer layer.

For sapphire or silicon substrates, a low temperature GaN, AlN or AlGaN buffer

15   may be grown.

As shown in FIG. 3, an AlGaN buffer layer 12 may be grown vertically from the mask openings 6 using a vapor phase epitaxy (VPE) technique such as hydride vapor phase epitaxy (HVPE), or more preferably metal-organic vapor phase epitaxy (MOVPE). In a preferred embodiment, the buffer layer 12 is grown to a thickness larger than the

20   thickness of the mask layer 14. Once the buffer layer 12 has been grown to a desired thickness, the epitaxial layer 20 is then grown by VPE, preferably in the same run or step as the buffer layer was grown.

As shown in FIG. 3A, epitaxial layer 20 grows laterally (i.e. parallel to the face of the substrate) in addition to vertically. Lateral growth fronts 22 move across the surface

25   of the mask stripes 14 as layer 20 grows.

Referring again to FIG. 3, in one embodiment, epitaxial layer 20 grows laterally until the growth fronts 22 coalesce at interfaces 24 to form a continuous layer 20 of gallium nitride. However, it is not necessary for the growth fronts to coalesce for all applications, as it is possible to fabricate devices in laterally overgrown portions of GaN

30   even if they have not coalesced with adjacent portions. As illustrated in FIG. 9, a useful portion of layer 20 may be fabricated without coalescence of adjacent portions. For

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example, a laser diode stripe may be fabricated in a region of layer 20 that has not coalesced. For fabrication of an LED, a coalesced layer is preferred. For example, an LED device 250μ wide and 275μ long may be fabricated on a coalesced layer of gallium nitride grown in accordance with the present invention.

5   The buffer layer 12 and the overgrown layer 20 may be grown using trimethylgallium (TMG), trimethylaluminum (TMA) and ammonia (NH_3) precursors in a diluent of H_2. A suitable MOVPE growth technique is described in greater detail in T. Weeks et al., "*GaN thin films deposited via organometallic vapor phase epitaxy on α(6H)-SiC(0001) using high-temperature monocrystalline AlN buffer layers,*" Appl.

10   Phys. Let., Vol. 67, No. 3, July 1995, pp. 401-403.

While the layer 20 of gallium nitride is growing, nucleation and growth of polycrystalline $Al_xGa_{1-x}N$ 30 typically begins to occur on the exposed upper surfaces of mask stripes 14. As illustrated in FIG. 4, if the growth rate of $Al_xGa_{1-x}N$ on the masks is too high, the lateral growth of layer 20 will be interrupted, preventing it from forming a

15   desired width of laterally overgrown material, and/or preventing it from coalescing with adjacent regions. Essentially, the polycrystalline $Al_xGa_{1-x}N$ 30 on the mask grows vertically and blocks the lateral growth of the single crystal layer 20.

The present inventors have discovered that it is possible, by controlling the horizontal and vertical growth rates of layer 20, to avoid interruption of the laterally

20   growing layer 20 by the polycrystalline $Al_xGa_{1-x}N$ 30. By increasing the lateral growth rate of layer 20 relative to its vertical growth rate by a given amount depending on the geometry of the structure, it is possible to grow a layer 20 that will grow to a desired distance despite nucleation on the mask.

Stated differently, by maintaining a sufficiently high lateral growth rate relative to

25   the vertical growth rate of layer 20, nucleation on the mask need not be controlled, since layer 20 will overgrow any polycrystalline nucleation and growth on the mask.

As a particular example, it has been discovered that by maintaining a ratio of lateral growth rate to vertical growth rate of at least 1:1, it is possible to grow a laterally-overgrown GaN layer on a stripe having a width of 5μ in a pattern with a period of 30μ

30   from a nucleation layer having an Al concentration of about 10%. By maintaining a lateral/vertical growth ratio of 4:1, it is possible to grow a layer of GaN over a mask

having 25μ-wide stripes. As shown in FIG. 5, when the lateral growth rate is caused to exceed the vertical growth rate by a sufficient amount, the growth fronts of the layer 20 may coalesce before the polycrystalline AlGaN growing on the stripes 14a,b grow large enough to block them.

5   The mechanisms for controlling the relevant growth factors will now be described in detail. The lateral and vertical growth rates of the overgrown layer 20 are controlled by a number of factors. One controlling factor is the so called "fill factor", defined herein as the ratio of the window length (l) to the stripe period (p). For a given window length, a higher fill factor (i.e. a larger window length for a given period) results in a slower

10   vertical growth rate. Conversely, for a given window length, a lower fill factor results in an increased vertical growth rate. Other factors for controlling the lateral and vertical growth rates are growth temperature, source gas flow rates, source gas nitrogen/gallium ratio, and growth pressure.

        If desired, once the laterally growing growth fronts 22 of the layer 20 have

15   coalesced over the masks, the growth conditions can be adjusted to increase the vertical growth rate.

        Although dependent on the structure of the particular epitaxial growth reactor being employed, typical growth parameters for the rates described herein are summarized in the following table.

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Parameter	Value
Growth temperature	1060-1120°C
Growth pressure	50-200 Torr
N/Ga ratio	2500
Fill factor	0.714 - 0.833
Lateral growth rate/vertical growth rate	1 - 4.2

Table 1 - Typical growth parameters.

        Preferably, a lateral growth rate of about 2-8 μ/hr and a vertical growth rate of about 1-2 μ/hr should be selected. A lateral growth rate of 6.3 μ/hr and a vertical growth rate of 1.5 μ/hr (4.2:1 ratio) may be achieved by growing the layer 20 by MOVPE at

25   1110°C and 200 Torr on a patterned mask of Si_xN_y stripes having a stripe width of 10μ, a

window width of 25μ and a period of 35μ for a fill factor of 0.71. The N/Ga ratio during growth of the layer 20 is preferably about 2500. Ratios of lateral growth rate to vertical growth rate may exceed 4.2:1.

To grow the buffer layer, TMG may flowed at $34.8\mu mol/min$, TMA may be
5   flowed at $6.5\mu mol/min$ and ammonia may be flowed at a rate of 10 slpm in a diluent of H_2 at 15.5 slpm. Once the buffer layer has been grown to a desired thickness, the layer 20 may be grown by flowing TMG at 309 $\mu mol/min$ and ammonia at a rate of 17 slpm in a diluent of H_2 at 22.5 slpm until the GaN layer has grown to a desired thickness.

A lateral and vertical growth rate of 4.2 μ/hr (1:1 ratio) may be achieved by
10   growing the layer 20 by MOVPE at 1060°C and 200 Torr on a patterned mask of Si_xN_y stripes having a stripe width of 10μ, a window length of 25μ and a period of 35μ for a fill factor of 0.71. The N/Ga ratio during growth of the layer 20 is preferably about 2500. It will be appreciated that other ratios, including ratios greater than 4.2:1, may be achieved through selection of other growth parameters.

15   An embodiment of the present invention utilizing pendeoepitaxial growth is illustrated in FIG. 6. In this embodiment, the substrate 10 is etched to form at least one raised portion 15, which defines adjacent recessed areas or trenches 18 on the substrate 10. FIG. 6 illustrates an embodiment in which a pair of raised portions 15a, 15b have been patterned using standard photolithographic techniques and reactive ion etching.
20   Preferably, the height of raised portions 15 (i.e. the depth of trenches 18) is at least 1μ. A mask layer 14, which may be Si_xN_y, SiO_2 or any other suitable mask is then deposited on the upper surface of substrate 10, with mask openings 16 made on the upper surfaces of raised portions 15a, 15b.

In this embodiment, the substrate 10 may be silicon carbide, sapphire, silicon,
25   gallium arsenide, gallium nitride or another Group III-nitride such as aluminum nitride or aluminum gallium nitride. The fabrication of aluminum nitride substrates is described in U.S. Patent No. 5,858,086 and 5,954,874 to Hunter, the disclosures of which are hereby incorporated herein by reference. Gallium nitride substrates have been fabricated by growing thick epitaxial layers of gallium nitride on a non-GaN substrate. Other methods
30   of obtaining gallium nitride substrates are summarized in A. Usui, et al., "Thick GaN epitaxial growth with low dislocation density by hydride vapor phase epitaxy," Jpn. J.

Appl. Phys. Vol. 36, pp. L899-902 (1997). It will be appreciated by those of skill in the art that when the substrate is a Group III-nitride, homoepitaxial growth may be used.

As shown in FIG. 6, if a buffer layer is required, an AlGaN buffer layer 12 may be grown vertically from the mask openings (or windows) 16 using MOVPE. In a preferred embodiment, the buffer layer 12 is grown to a thickness larger than the thickness of the mask layer 14. Once the buffer layer 12 has been grown to a desired thickness, the pendeoepitaxial layer 26 is then grown. Pendeoepitaxial layer 26 grows laterally (i.e. parallel to the face of the substrate) over trenches 18 in addition to vertically.

Although nucleation and growth of polycrystalline GaN 30 may be occurring on the mask 14, it is occurring within trenches 18, and thus does not interfere with the lateral growth of pendeoepitaxial layer 26.

FIG. 12 is a cross sectional SEM of a pendeoepitaxial GaN layer grown in accordance with this embodiment of the invention. Polycrystalline AlGaN material is evident within the trench, but does not interfere with the lateral growth of the GaN layer.

It will be readily appreciated that a trench depth of 1μ is exemplary. Trenches 18 may be fabricated with depths less than or greater than 1μ if desired or necessary depending on the rate of polycrystalline growth on the mask or the width of the pendeoepitaxial layer to be grown.

In one embodiment, pendeoepitaxial layer 26 grows laterally until opposing growth fronts 22 coalesce at interfaces 24 to form a continuous layer 26 of gallium nitride. However, as mentioned above, it is not necessary for the growth fronts 22 to coalesce for all applications, as it is possible to fabricate devices in laterally overgrown portions of GaN even if they have not coalesced with adjacent portions.

FIG. 13 is a plan view SEM image of two pendeoepitaxial GaN stripes grown in accordance with this embodiment of the present invention.

For the embodiment illustrated in FIG. 6, alternative methods of forming the mask layer 14 are illustrated in FIGs 6A and 6B. As discussed above, raised portions 15 may be formed using standard etching techniques. Typically, this involves patterning the surface of a substrate with an etch mask, etching the substrate to the desired depth, and then removing the etch mask. As shown in FIG. 6A, after the etch mask has been

removed, the mask layer 14 may be formed on the surface of substrate 10 by PECVD. Windows 16 are then opened in mask 14 to reveal the upper surfaces of raised portions 15.

Because of the tolerance limitations of photolithographic techniques, when the windows 16 are opened in mask 14, it is difficult to align the edges of windows 16 with the edges of raised portions 15. Thus, there is some overlap 17 of the mask 14 onto the upper surfaces of raised portions 15.

A simplified method of forming mask 14 is illustrated in FIG. 6B. In this method, an etch mask 19 is applied to the surface of substrate 10, and substrate 10 is etched to form trenches 18. Mask 14 is deposited after etching trenches 18 but prior to removing etch mask 19. In this technique, mask 14 preferably comprises a thin mask layer of about 50-200 Å in thickness. Mask 14 may comprise Si_xN_y, SiO_2, or any other suitable mask material. Etch mask 19 is then removed, revealing the upper surfaces of raised portions 15. The edges of windows 16 in mask 14 are thereby self-aligned with the edges of raised portions 15. Thus, with this technique, only a single masking step is required and it is not necessary to use photolithographic techniques to open windows 16 in mask layer 14.

FIG. 7 is a cross-sectional SEM image showing the interruption of lateral growth of a GaN layer by crystals nucleating on the mask.

FIG. 8 is a plan view SEM image of two GaN stripes in which crystallites on the underlying mask disturbed the epitaxial growth.

FIG. 9 is a cross-sectional SEM of GaN stripes grown in accordance with an embodiment of the present invention using a reflector mask layer.

FIG. 10 is a cross-sectional SEM of GaN stripes grown in accordance with an embodiment of the present invention until adjacent regions have coalesced over the masks.

FIG. 11 is a cross-sectional SEM of a GaN layer grown on a conductive buffer layer over a Si_3N_4 mask.

FIG. 14 is a cross-sectional TEM (Transmission Electron Microscopy) image of a layer of GaN grown in accordance with the present invention. The defect densities

observed indicate an estimated reduction from approximately $10^9/cm^2$ in the regions over the windows to approximately $10^6/cm^2$ in the regions above the mask stripes.

Example 1:

A patterned mask of Si_xN_y stripes having a stripe width of 10μ, a window length of 25μ and a period of 35μ for a fill factor of 0.715 was applied to a 6H-SiC substrate. The stripes were arranged parallel to the $<1\bar{1}00>$ direction. A 0.5μ thick $Al_{0.1}Ga_{0.9}N$ buffer layer was grown by MOVPE by flowing TMG at $34.8\mu mol/min$, TMA at $6.5\mu mol/min$ and ammonia at 10 slpm in a diluent of H_2 at 15.5 slpm at 1020°C and 76 Torr for a total of 80 minutes. Following growth of the buffer layer, an epitaxial layer of GaN was grown by MOVPE by flowing TMG at $309 \mu mol/min$ and ammonia at 17 slpm in a diluent of H_2 at 22.5 slpm at 1110°C and 200 Torr for 45 minutes. The ratio of lateral to vertical growth under these conditions was approximately 4.2:1. FIG. 15 is an SEM image a cross section of the resulting GaN layer.

Example 2:

A patterned mask of Si_xN_y stripes having a stripe width of 10μ, a window length of 25μ and a period of 35μ for a fill factor of 0.715 was applied to a 6H-SiC substrate. The stripes were arranged parallel to the $<1\bar{1}00>$ direction. A 0.5μ thick $Al_{0.1}Ga_{0.9}N$ buffer layer was grown by MOVPE by flowing TMG at $34.8\mu mol/min$, TMA at $6.5\mu mol/min$ and ammonia at 10 slpm in a diluent of H_2 at 15.5 slpm at 1050°C and 76 Torr for a total of 80 minutes. Following growth of the buffer layer, an epitaxial layer of GaN was grown by MOVPE by flowing TMG at $309 \mu mol/min$ and ammonia at 17 slpm in a diluent of H_2 at 22.5 slpm at 1060°C and 200 Torr for one hour. The ratio of lateral to vertical growth under these conditions was approximately 1:1. FIG. 16 is an SEM image a cross section of the resulting GaN layer.

In the specification and drawings, there have been set forth preferred and exemplary embodiments of the invention which have been included by way of example and not by way of limitation, the scope of the invention being set forth in the accompanying claims.